

Development of Increased Reliability Vertical Cavity Surface Emitting Laser Arrays

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Project Goals

- Development of high reliability two-dimensional VCSEL arrays via minimization of thermal impedance, particularly at 40 Gbit/second data rates.

Technical Approach

- Use of flip-chip bonded VCSELs in which the bump conveys the heat into the host substrate. Minimization of thermal impedance via shortening of top mirror stack while maintaining low current threshold. Mirror stack shortening is facilitated by use of top high-adhesion gold contact. First result of study will be plot of thermal impedance vs. threshold current as number of mirror pairs is varied.

Accomplished Milestones

- We have achieved ~ 500 K/W thermal impedance but not demonstrated reliable operation of this device due to its simple design, which has a mesa etched through the active region leading to high surface recombination velocity and associated defect propagation. For reliable design, a trench-mesa construction must be used, with additionally offset contacting to the buried n-layer, to reduce this free-surface defect source. Concurrently, we have measured the reliability of commercial flip-chip designs and found that the mechanical stress induced by the flip-chip bonding leads to ~ two orders of magnitude decrease in lifetime. The scientific and engineering quandary is how to achieve the low thermal impedance of close bonding to the active region, without inducing higher failure rates at a given temperature. Additionally, figure 1 shows that thermal impedance must further be reduced to ~ 100 K/W for reliable 40 Gbit/second operation.

Near-Term Milestones

- In further near-term study, we intend to construct trench-mesa VCSEL's at our current thermal impedance target of 500 K/W and repeat the lifetime study performed with the commercial flip-chip devices, hopefully closing the circle data point shown in figure 1.

Long-Term Milestones

- The medium term milestone is to then reduce thermal impedance of our flip-chip bonded VCSEL's to 100 K/W using better materials and device design, which should place us at a lifetime of ~ 250 hours at 40 Gbit/second. The long term milestone is to deduce the physical phenomena directly responsible for the increase failure rate due to flip-chip bonding and eliminate it, increasing lifetime to ~ 25000 hours at 40 Gbit/second, or 3 years.

Demonstration Activity

➤ See figure 1.

INSERT GRAPHICS HERE

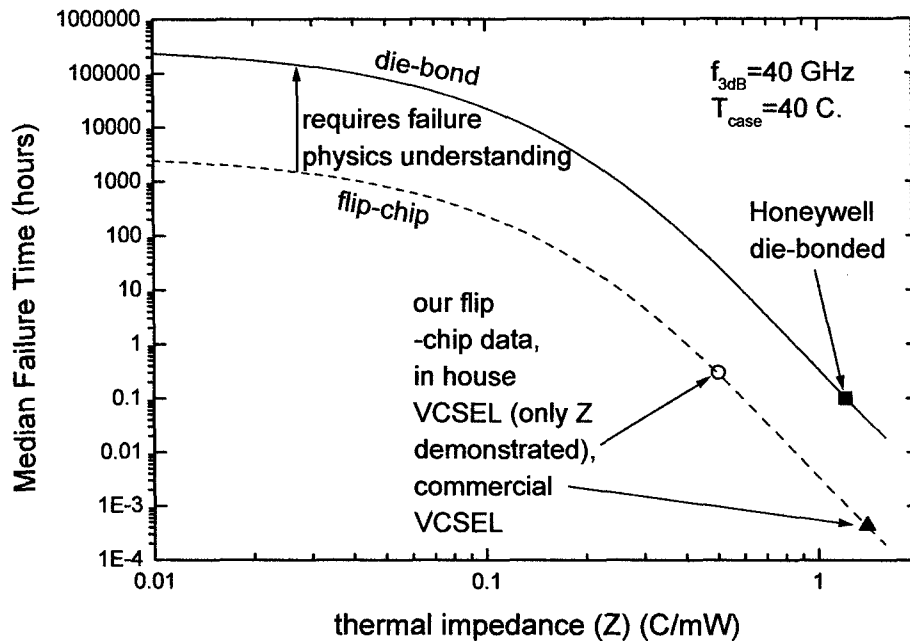


Figure 1: Plot of Median Failure Time of VCSEL's with -3dB frequency of 40 GHz vs. thermal impedance, showing the marked effect of thermal considerations on lifetime. The square indicates current commercial availability in die-bonded packaging. The triangle shows our results with commercially available flip-chip vcsels, and indicated on the plot by the dashed line is the detrimental effect flip-chip bonding has on reliability at a given temperature, due to internal stresses caused by the bonding. The open circle shows our best thermal impedance device, for which associated reliability is not yet determined (due to the simple nature of the device design which is not made for reliability), projected onto this dashed curve. So, to achieve reliable 40 Gbit/second data rates using VCSEL's, (1) low thermal impedance must be achieved using flip-chip bonding without associated detrimental stress effects, and (2) thermal impedance must yet be reduced through more exotic device design.

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13. ABSTRACT (Maximum 200 words) Vertical Cavity Surface Emitting Lasers (VCSEL's) should see increasing use for short distance optical interconnects in the next 5-10 years -- data rate requirements will exceed 10 Gbit/second. It was shown in the proposal that at these data rates electrical current requirements on the VCSELs cause excessive failure rates due to current mitigated defect formation and thermal rise in the active region. Here the thermal rise is addressed through reduction of thermal impedance from the active region to the heat sink. For 40 Gbit/second VCSELs, a reduction of thermal impedance from 1500 C/W to 100 C/W will increase mean lifetime from minutes to years. We proposed to achieve this reduction via flip-chip bonding of the VCSEL, using solder bonding directly to the VCEL's active area, in conjunction with a reduction of the associated mirror stack via incorporation of metal reflectors. We have achieved 500 C/W, albeit with increased failure rate at a given active region temperature due to bond stresses. This quandary of being able to reduce thermal impedance by bonding near the active region to provide a direct heat path, but at the same time increasing failure rate at a given temperature because of the mechanical stresses induced needs to be addressed in future work.					
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